NOTES:(UNLESS OTHERWISE SPECIFIED)

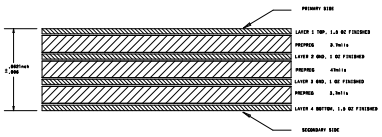
1. RoHS COMPLIANT CERTIFICATION OR MATERIAL DECLARATION REQUIRED
2. MATERIAL:
   A. IS410 OR EQUIVALENT. MATERIAL MUST CONFORM TO UL94V-0.
   B. USE HTE COPPER, AS SPECIFIED IN THE CROSS SECTION DIAGRAM.
   C. OVERALL METAL TO METAL THICKNESS AS SPECIFIED IN THE CROSS SECTION
3. DRILLING:
   A. DIAMETERS IN DRILL TABLE ARE FINISHED HOLE SIZES +/-.003 TOL.
      UNLESS OTHERWISE SPECIFIED IN DRILL TABLE.
   B. TEARDROP ALLOWED ON ENTRY OF VIA ON EVERY TRACE LAYER.
4. PLATING:
      COPPER PLATING IN THRU-HOLES .001 min.
5. MARKING:
   A. SILKSCREEN IN WHITE NON-CONDUCTIVE EPOXY INK ON PRIMARY SIDE OF THE
      BOARD OR BOTH SIDES IF APPLICABLE.
6. FINAL FABRICATION:
   A. SOLDERMASK PRIMARY AND SECONDARY SIDE OF BOARD USING LIQUID PHOTOIMAGABLE
      MASK MATERIAL OVER BARE COPPER..PER IPC-SM-840. MASK ARTWORKS PROVIDED
      ARE 1:1. SOLDERMASK COLOR **BLUE**
   B. ALL VIAS THAT ARE PLACED ON EXPOSED PADS MUST BE PLUGGED WITH SOLDERMASK INK ON THE SIDE
      WHERE IT IS MASKED IN THE SOLDER MASK FILM.THIS IS TO AVOID SOLDER FLOW THROUGH VIA HOLE.
7. FINISH:
   A. SHALL BE ELECTROLYTIC NICKEL/GOLD. ELECTROLESS NIKEL / IMMERSION GOLD. (ENIG)
   B. NICKEL THICKNESS. 100-200 MICROINCHES.
   C. GOLD THICKNESS: 3-10 MICROINCHES.
8. BOARDS SHALL BE PURCHASED FROM UL RECOGNIZED VENDORS ONLY AND SHALL BE
   MARKED IN COPPER ON SECONDARY SIDE OF BOARD WITH VENDORS UL IDENT.
   FLAMABILITY RATING (94-V), DATE CODE (WWYY), AND RoHS COMPLIANT SYMBOL.
9. MANUFACTURE BOARD TO BE IN ACCORDANCE WITH PERFORMANCE STANDARD
   IPC-6011/6012 CLASS 2 BOARD TO BE INSPECTED PER IPC-600-A CLASS 2.
10. MAXIMUM WARP OR TWIST SHALL NOT EXCEED 0.005" PER INCH

11. TESTING:

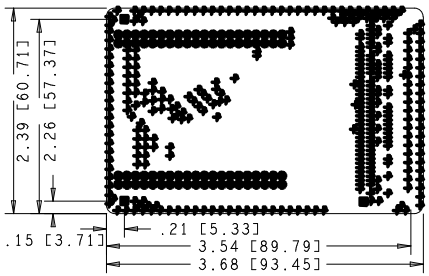
A. FABRICATOR TO ADD TEST STRUCTURES OR COUPONS AS NEEDED
B. T-LINE IMPEDANCE TO BE TESTED OR GURANTEED WITHIN 10% IF SPECIFIED IN
   THE CROSS SECTION. TOLERANCE TO BE +/-10% UNLESS OTHERWISE SPECIFIED

12. LAYER LADDER PROVIDED IN THE PCB SHOULD NOT BE MASKED

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
1	INITIAL RELEASE	11/04/14	
2	NETNAME CHANGE DELETION OF TWO MOUNTING HOLES	15/05/14	
3	FIXED DFA ISSUES	05/06/14	



SECTION A-A
SCALE: NONE
(X-SECTION VIEW / 4 LAYER BOARD)



DRILL CHART: TOP to BOTTOM ALL UNITS ARE IN MILS				
FIGURE	SIZE	TOLERANCE	PLATED	QTY
✦	12.0	+3.0/-3.0	PLATED	340
●	39.37	+3.0/-3.0	PLATED	80
■	50.0	+2.0/-2.0	NON-PLATED	2
■	118.0	+2.0/-2.0	NON-PLATED	2

SINGLE ENDED

LAYER NO.	CONDUCTOR WIDTH	REFERENCE LAYER	IMPEDANCE +/-10%
LAYER 1	5.65 Mils	2	50-ohm +/-10%
LAYER 4	5.65 Mils	3	50-ohm +/-10%

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHS [mm]
TOLERANCES ON; ANGLES +/- 2°
2 PL DECIMALS +/- .010
3 PL DECIMALS +/- .005
THIRD ANGLE PROJECTIONS

SIGNATURES		DATE
DRAWN	: SRIRAMAN	05/06/2014
CHECKED	: PRAJITH	05/06/2014
ENGINEER	: SHREESHA	05/06/2014
ISSUED		

CYPRESS PROPRIETARY
THIS DOCUMENT CONTAINS CONFIDENTIAL, PROPRIETARY INFORMATION THAT IS CYPRESS SEMICONDUCTOR PROPERTY. DO NOT DISCLOSE TO OR DUPLICATE FOR OTHERS EXCEPT AS AUTHIRIZED BY CYPRESS.

COMPANY: CYPRESS SEMICONDUCTOR
198 CHAMPION COURT
SAN JOSE, CA 95134
(408) 943-2600

FABRICATION DRAWING
CYUSB3ACC-005
FMC Interconnect Board

SIZE	FSCM NO	DWG NO	REV
C		610-60192-01	03

SCALE: 1/1 SHEET: 1 OF 1